Silicon Mountain
MEMORY®

www smmdirect.com

128MB, PC133 DIMM, Unbuffered, 16 x 64bit

Specifications

- PC133/7.5ns cycle time support
- 168 pin unbuffered DIMM
- 4 SDRAM internal banks
- 1 module bank
- 4096 refresh cycles (4k refresh)
- Auto and Self refresh
- LVTTL (3.3 volt) I/O interface
- DQM data mask
- Serial Presence Detect via onboard EEPROM
- Programmable CAS (read) latency 3
- 1,2,4,8, and Full Page burst lengths supported
- Internal pipelined operation

General Description

The SMIB44846/128 is a JEDEC compliant 128MB DIMM constructed on a 168 pin, 6-layer glass-epoxy PCB. Its memory consists of eight 16M x 8bits CMOS DRAMS in a 400mil, 54pin, TSSOP II package. On board is one 2Kbit EEPROM in an 8pin, TSSOP package that contains the SPD read by the memory controller.

This module is designed for the interchange of 128Mbytes of data and all inputs and outputs are fully synchronized at the rising edge of the clock cycle. All DRAM and module banks are capable of being addressed with interleaved technology.

address 4755 walnut street boulder, colorado 80301 usa
tele 888.745.6866 fax 303.938.1166