

1GB DDR SDRAM SO-DIMM (2100, 2700, 3200)

Specifications

- 200-pin, small-outline, dual in-line memory module (SODIMM)
- 1GB (128 Meg x 64)
- VDD = VDDQ = +2.6V
- 2.6V I/O (SSTL_2 compatible)
- VDDSPD = +2.3V to +3.6V
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bi-directional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs CK and CK#
- Four internal device banks for concurrent operation
- Programmable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes
- 7.8125µs maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Programmable READ CAS latency
- Gold edge contacts

General Description

The 1GB DDR SDRAM SO-DIMM (2100, 2700, 3200) is a high-speed CMOS, dynamic random-access, 1GB memory modules organized in a x64 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAM devices.

DDR SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR SDRAM module effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bi-directional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for

READs and center-aligned with data for WRITEs.

DDR SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA₀, BA₁ select device bank; A₀–A₁₂ select device row). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable read or write burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL₂. All out-puts are SSTL₂, Class II compatible.