

## 256MB DDR SDRAM SO-DIMM (2100, 2700, 3200)

### Specifications

- 200-pin, small-outline, dual in-line memory module (DDR SODIMM)
- Utilizes 266 MT/s and 333 MT/s DDR SDRAM components
- 256MB (32 Meg x 64)
- VDD= VDDQ= +2.5V
- VDDSPD = +2.3V to +3.6V
- 2.5V I/O (SSTL\_2 compatible)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Bidirectional data strobe (DQS) transmitted/received with data—i.e., source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Four internal device banks for concurrent operation
- Selectable burst lengths: 2, 4, or 8
- Auto precharge option
- Auto Refresh and Self Refresh Modes 7.8125µs
- 256MB maximum average periodic refresh interval
- Serial Presence Detect (SPD) with EEPROM
- Selectable READ CAS latency for maximum compatibility
- Gold edge contacts

### General Description

The modules are high-speed CMOS, dynamic random-access 256MB memory modules organized in x64 configuration. DDR SDRAM modules use internally configured quad-bank DDR SDRAMs.

DDR SDRAM modules use a double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 2n-pre-fetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for DDR SDRAM modules effectively consists of a single 2n-bit wide, one-clock-cycle data transfer at the internal DRAM core and two corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

A bi-directional data strobe (DQS) is transmitted externally, along with data, for use in data capture at the receiver. DQS is an intermittent strobe transmitted by the DDR SDRAM during

READs and by the memory controller during WRITES. DQS is edge-aligned with data for READs and center-aligned with data for WRITES.

DDR SDRAM modules operate from differential clock inputs (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands (address and control signals) are registered at every positive edge of CK. Input data is registered on both edges of DQS, and out-put data is referenced to both edges of DQS, as well as to both edges of CK.

Read and write accesses to DDR SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA<sub>0</sub>, BA<sub>1</sub> select device bank; A<sub>0</sub>–A<sub>11</sub> select device row for 64MB, A<sub>0</sub>–A<sub>12</sub> select device row for 128MB, 256MB). The address bits registered coincident with the READ or WRITE command are used to select the device bank and the starting device column location for the burst access.

DDR SDRAM modules provide for programmable READ or WRITE burst lengths of 2, 4, or 8 locations. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst access.

The pipelined, multibank architecture of DDR SDRAM modules allows for concurrent operation, thereby providing high effective bandwidth by hiding row precharge and activation time.

An auto refresh mode is provided, along with a power-saving power-down mode. All inputs are compatible with the JEDEC Standard for SSTL<sub>2</sub>. All out-puts are SSTL<sub>2</sub>, Class II compatible.