

512MB, PC133 DIMM, Unbuffered, 64 x 64bit

Specifications

- PC133/7.5ns cycle time support
- 168 pin unbuffered DIMM
- 4 SDRAM internal banks
- 2 module banks
- 8192 refresh cycles (8k refresh)
- Auto and Self refresh
- LVTTTL (3.3 volt) I/O interface
- DQM data mask
- Serial Presence Detect via onboard EEPROM
- Programmable CAS (read) latency 3
- 1,2,4,8, and Full Page burst lengths supported
- Internal pipelined operation

General Description

The 512MB, PC133 DIMM, Unbuffered, 64 x 64bit is a JEDEC compliant 512MB DIMM constructed on a 168 pin, 6-layer glass-epoxy PCB. Its memory consists of sixteen 32M x 8bits CMOS DRAMS in a 400mil, 54pin, TSSOP II package. On board is one 2Kbit EEPROM in an 8pin, TSSOP package which contains the SPD read by the memory controller.

This module is designed for the interchange of 512Mbytes of data and all inputs and outputs are fully synchronized at the rising edge of the clock cycle. All DRAM and module banks are capable of being addressed with interleaved technology.