

512MB, PC2700 DDR DIMM, Unbuffered, 64 x 64bit

Specifications

- PC2700/5.0ns cycle time support
- CAS latency 2.5 support
- 184 pin unbuffered non-ECC DIMM
- 4 SDRAM internal banks
- 2 module banks
- 8192 refresh cycles (8k refresh)
- Auto and Self refresh
- SSTL_2 (2.5 volt) I/O interface
- DQM data mask
- Serial Presence Detect via onboard EEPROM
- Programmable CAS (read) latencies of 2.0/2.5/3.0
- Programmable 1,2,4, and 8 burst lengths supported
- Internal pipelined operation

General Description

The 512MB, PC2700 DDR DIMM, Unbuffered, 64 x 64bit is a JEDEC compliant 512MB DIMM constructed on a 184 pin, 6-layer glass-epoxy PCB. Its memory consists of sixteen 32M x 8bits CMOS DRAMS in a 400mil, 66pin, TSOP package. On board is one 2Kbit EEPROM in an 8pin, TSSOP package which contains the SPD read by the memory controller.

This module is designed for the interchange of 512Mbytes of data and all inputs and outputs are fully synchronized at the rising and falling edges of the clock cycle. All DRAM and module banks are capable of being addressed with interleaved technology.